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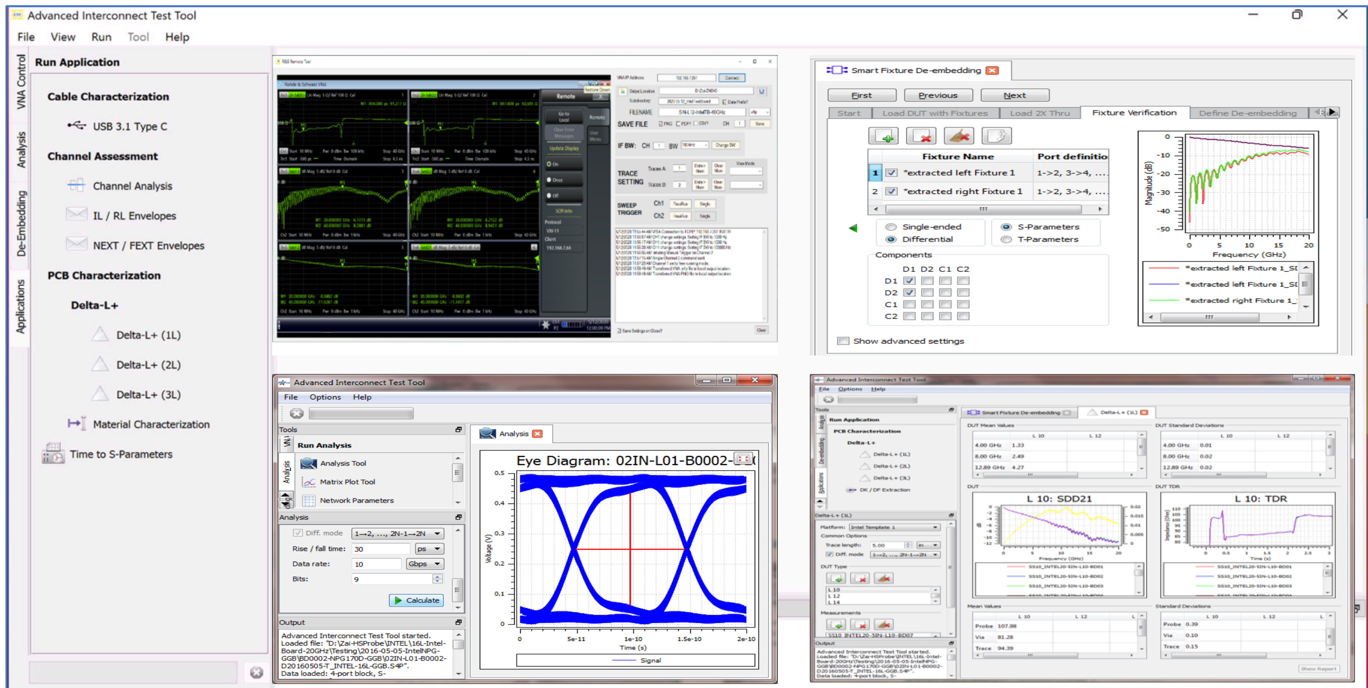
Advanced Interconnect Test Tool (AITT)

Versatile Tool for Interconnect Analysis and PCB Characterization



AITT Overview

The Advanced Interconnect Test Tool (AITT) is ideal for signal-integrity and power-integrity applications. The AITT software includes the key features: de-embedding, applications including PCB material extraction, analysis tools, and VNA control. It can be installed on a VNA directly or a PC that controls the VNA remotely.

The Advanced Interconnect Test Tool (AITT) is developed by an experienced research team led by two IEEE Fellows in the Missouri S&T EMC Laboratory. This versatile, easy-to-use AITT software has been used by many Fortune 100 companies.

Part Numbers:

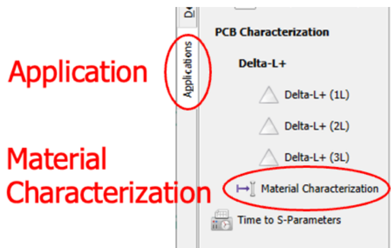
AITT-AN: Analysis Tool
AITT-SFD: Analysis Tool and Smart Fixture De-embedding Tool
AITT-DLP: Analysis Tool and Delta-L+ Tool
AITT-ME: Analysis Tool and Material Extraction Tool (DK, DF, and surface roughness)

Features:

- **Smart Fixture De-embedding**: multiport fixture de-embedding tool supports 2X thru and 1X reflect techniques with superior accuracy.
- **Analysis**: powerful tool for frequency- domain, time-domain, and eye-diagram analysis, and versatile plotting capabilities.
- **Causality/Passivity:** tool assesses the causality and passivity of an S-parameter file and can enforce them for non-causal or non-passive cases.
- **VNA Control**: control of a VNA locally or remotely by a separate computer.
- **Applications**:
  - PCB Material Extraction tool extracts DK, DF, and surface roughness of PCBs.
  - Delta-L 4.0 PCB test tool is based on the Intel Delta-L 4.0 methodology
- **Fast** C++ runtime with simple installation and script-mode support.

Material Characterization (AITT-ME) Tool

The AITT-ME material extraction tool extracts DK, DF, and surface roughness of a PCB from trace measurements based on the Huray roughness model. DK for both pre-preg and core can be extracted from stripline measurements as well.



The input can be defined as single-ended or differential trace with single or dual mode, or DUT data with 2xThru can be used, where the SFD algorithm will be applied for de-embedding before material extraction. The Intel Extended Unterminated Line (EUL) method is used to extract both core and pre-preg DK.

THRU Structure

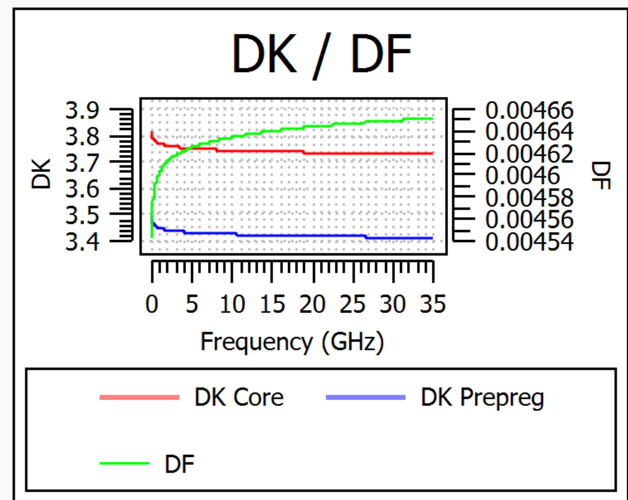
Trace type:	○ Single-ended	◉ Differential
Calculate from:	◉ 2 line structure	○ DUT
Total structure:	DeltaL.s4p	
2x THRU:		
	☑ Fixture autocorrection	
Port order:	1->2, 3->4, ... , 2N-1->2N	
DUT length:	8	in

The input stack-up can be developed by putting various geometry parameters, such as trace width, core and pre-preg height, thickness, spacing, and conductivity.

Stackup

Trace long width ($W_{l,THRU}$):	5.2	mil
Trace short width ($W_{s,THRU}$):	4.8	mil
Trace spacing (S_{THRU}):	6.2	mil
Prepreg height (H_{pg}):	5	mil
Core height (H_{co}):	4	mil
Trace thickness (T):	1.1	mil
Copper conductivity:	4.70e+07	S/m

Results for DK pre-preg and core, DF and surface roughness level are given.



The application gives the common-mode and differential mode insertion losses and comparison of measurement with simulation.